MOS VARACTOR USING ISOLATION WELL

DESCRIPTION

[Para 1] Field of the Invention

[Para 2] The present invention relates to complementary metal oxide semiconductor (CMOS) and bipolar/CMOS (BiCMOS) electronic devices that include a varactor that has improved tunability which, in some instances, can enable negative biasing and isolation that reduces noise, e.g., parasitics, as well as a process for fabricating such devices. The inventive electronic devices, which include the varactor, are highly suitable for use in mobile or cellular phones, personnel digital assistances (PDAs) and other high RF (radio frequency) electronic devices.

[Para 3] Background of the Invention

[Para 4] Varactors are electronic devices that have a capacitance that is controlled by a suitable voltage or current bias. Varactors are typically employed, for example, in so-called voltage controlled oscillators (VCOs) where a frequency of an oscillator is controlled by an applied current or voltage. In such instances, the VCOs are used when a variable frequency is required, or when a signal needs to be synchronized to a reference signal.

[Para 5] In radio communication devices, such as mobile/cellular phones, VCOs are typically employed in phase locked loop circuits to generate suitable signals including: generation of a reference signal that is synchronized with a signal received by a radio receiver, modulation/demodulation operations and

frequency synthesis.

[Para 6] Numerous varactors have been developed and are successfully employed in integrated circuit technologies. For example, it is known to employ pn-diodes, Schottky diodes or MOS-diodes as a varactor in bipolar, CMOS and BiCMOS technologies. In the article to R. A. Moline, et al., entitled "Ion-Implanted Hyperabrupt Junction Voltage Variable Capacitors" IEEE Trans. Electron. Device, ED-19, pp267f, 1972, varactors comprising pn-diodes are described. U.S. Pat. No. 3,638,300 to Foxhall, et al.; U.S. Pat. No. 4,226,648 to Goodwin, et al.; U.S. Pat. No. 4,827,319 to Pavlidis, et al; and U.S. Pat. No. 5,557,140 to Nguyen, et al. describe other types of variable capacitor (i.e., varactor) diodes that include hyper-abrupt ion-implanted junctions. The term `hyper-abrupt` denotes that the implant has a doping profile that is in contact with the wall of the adjacent extrinsic base region. U.S. Pat. No. 4,973,922 to Embree, et al.; U.S. Pat. No. 5,965,912 to Stolfa, et al; and U.S. Pat. No. 6,100,770 to Litwin, et al., on the other hand, describe MOS-diodes that are employed as varactors.

[Para 7] The integration of varactors depends on the capability of the integrated circuit technology. An overview of integrated circuit devices for high RF applications in BiCMOS technology is described, for example, in J. N. Burghartz, et al. "Integrated RF and Microwave Components in BiCMOS Technology", IEEE Trans. Electron Devices, Col. 43, pp1559, September 1996. As is stated therein, varactors are not a part of the standard BiCMOS device set. Instead, it is proposed to employ a collector-base junction of a bipolar transistor as a varactor.

[Para 8] In order to use a device as a varactor, the device must satisfy one or more, preferably two or more, of the following criteria: (1) tunability (i.e., ratio of maximum capacitance to minimum capacitance) must be high (on the order of about 3 or greater); (2) Quality factor Q must be high (on the order of about

20 or greater); and (3) the device must exhibit linearity.

[Para 9] Many of the known prior art varactors do not meet the above criteria. For example, traditional base-collector junction varactors rely on the NPN base-collector profile, which is not optimized for varactor tunability. In the case of hyper-abrupt base-collector junction varactors, where the doping profile of the implant is located at the "wall" of the extrinsic base region, the device lacks linearity. With traditional MOS varactors, the tunability is high; however, an even higher tunability is often required.

[Para 10] In view of the above-mentioned drawbacks with prior art varactors, there is a continued need for providing new and improved varactors, which satisfy the above criteria and that can be integrated with CMOS and BiCMOS devices.

[Para 11] Moreover, in conventional MOS varactor designs it is difficult to electrically isolate the MOS varactor from the bulk substrate. The lack of sufficient electrical isolation results in a device that has high parasitics, e.g., noise. As such, there is also a need to provide a varactor design that has sufficient electrical isolation thereby reducing noise in the device.

[Para 12] Summary of the Invention

[Para 13] The present invention provides a varactor that has increased tunability and a high quality factor Q as well as a method of fabricating the varactor. The method of the present invention can be integrated into a conventional CMOS processing scheme or into a conventional BiCMOS processing scheme.

[Para 14] Specifically, and in broad terms, the varactor of the present invention comprises:

[Para 15] a semiconductor substrate of a first conductivity type, said substrate including a doped region of a second conductivity type located below an upper region of said substrate, said first conductivity type is different, in terms of dopant type, from said second conductivity type;

[Para 16] a well region located in said upper region of said substrate, wherein said well region includes outer well regions of said second conductivity type and an inner well region of said first conductivity type, each well of said well region is separated at an upper surface by an isolation region; and

[Para 17] a field effect transistor having at least a gate conductor of said first conductivity type located above said inner well region.

[Para 18] In some embodiments in which a BiCMOS or a bipolar transistor is to be fabricated, the doped region of the second conductivity type is a subcollector. In other embodiments in which a CMOS device is to be fabricated, the doped region of the second conductivity type is an isolation well.

[Para 19] In one embodiment of the present invention, which represents a preferred embodiment, the varactor comprises

[Para 20] a p-type semiconductor substrate, said p-type substrate including an n-doped region, i.e., subcollector or isolation well, located below an upper region of said substrate;

[Para 21] a well region located in said upper region of said substrate, wherein said well region includes outer N-well regions and an inner P-well region, each well of said well region is separated at an upper surface by an isolation region; and

[Para 22] a field effect transistor having at least a p-type gate conductor located above said inner P-well region.

[Para 23] In another embodiment of the present invention, the varactor comprises

[Para 24] an n-type semiconductor substrate, said n-type substrate including a p-doped region, i.e., subcollector or isolation well, located below an upper region of said substrate;

[Para 25] a well region located in said upper region of said substrate, wherein said well region includes outer P-well regions and an inner N-well region, each well of said well region is separated at an upper surface by an isolation region; and

[Para 26] a field effect transistor having at least an n-type gate conductor located on said inner N-well region.

[Para 27] In addition to the varactor structure, the present invention also provides a method of fabricating the same. The method includes the steps of:

[Para 28] providing a structure that comprises a semiconductor substrate of a first conductivity type;

[Para 29] forming a plurality of isolation regions in said upper region of said substrate;

[Para 30] forming a well region in said upper region of said substrate, wherein said well region includes outer well regions of a second conductivity type that differs from the first conductivity type and an inner well region of said first conductivity type, each well of said well region is separated at an upper surface by an isolation region; and

[Para 31] forming a field effect transistor having at least a gate conductor of said first conductivity type above said inner well region.

[Para 32] In one embodiment, the substrate includes a doped region of a second conductivity type located below an upper region of the substrate. The doped region can be formed prior to forming the plurality of isolation regions or after forming the plurality of isolation regions, yet prior to well region formation. It is again noted that the doped region can be a subcollector for a BiCMOS or bipolar device, or an isolation well for a CMOS device.

[Para 33] In the case of a preferred varactor structure, the method includes the steps of:

[Para 34] providing a structure that comprises a p-type semiconductor substrate;

[Para 35] forming a plurality of isolation regions in said upper region of said substrate;

[Para 36] forming a well region in said upper region of said substrate, wherein said well region includes outer well N-regions and an inner P-well region, each

well of said well region is separated at an upper surface by an isolation region; and

[Para 37] forming a field effect transistor having at least a p-type gate conductor above said inner well region.

[Para 38] In one embodiment, the substrate includes a doped region of a second conductivity type located below an upper region of the substrate. The doped region can be formed prior to forming the plurality of isolation regions or after forming the plurality of isolation regions, yet prior to well region formation

[Para 39] Brief Description of the Drawings

[Para 40] FIGS. 1A-1D are pictorial representations (through cross sectional views) illustrating the basic processing steps employed in the present invention for fabricating an accumulation varactor for BiCMOS or bipolar applications.

[Para 41] FIG. 2 is a plot of CV characteristics (capacitance density vs. gate voltage Vg) for a prior art NMOS in a n-well (Curve 1), a prior art PMOS in a p-well (Curve 2), and the inventive PMOS accumulation varactor (Curve 3).

[Para 42] FIGS. 3A-3C are pictorial representations (through cross sectional views) illustrating the basic processing steps employed in the present invention for fabricating an accumulation varactor for CMOS applications.

[Para 43] Detailed Description of the Invention

[Para 44] The present invention, which provides a MOS varactor having improved tunability and reduced parasitics, i.e., noise, as well as a method of fabricating the same will now be described in greater detail by referring to the drawings that accompany the present application. It is noted that the drawings of the present application are provided for illustrative purposes and are thus not drawn to scale. Moreover, like and corresponding elements shown in the drawings are referred to by like reference numerals.

[Para 45] In the description that follows, a PMOS varactor for BiCMOS and bipolar applications including an alternating N-well, P-well, and N-well layout and a n-type subcollector is described. Although this arrangement is described in detail, the present invention also contemplates a NMOS varactor for BiCMOS or bipolar applications that would include an alternating P-well, N-well, and P-well layout and a p-type subcollector. The NMOS varactor is made by using the opposite dopant conductivity than the PMOS varactor. It is noted that for BiCMOS or bipolar applications such as shown, for example, in FIGS. 1A-1D, the subcollector, which represents a doped region of a second conductivity type that differs from the first conductivity type dopant present in the substrate, is present. In CMOS applications, an isolation well, which represents a doped region of a second conductivity type that differs from the first conductivity type dopant present in the substrate, is present. The dope region can be formed prior to the forming isolation regions or after isolation region formation, but prior to the inventive well region formation.

[Para 46] Reference is first made to FIG. 1A which illustrates an initial structure 10 that is formed after n+ subcollector 14 is formed into a portion of semiconductor substrate 12. The semiconductor substrate 12 comprises a semiconducting material including, for example, Si, SiGe, SiGeC, SiC, GaAs, InAs, InP or layered semiconductors such as, for example, silicon-on-insulators (SOIs), SiGe-on-insulators (SGOIs), and Si/SiGe. For the embodiment illustrated, the semiconductor substrate 12 is a p-type substrate. Note that the substrate 12 includes an upper region 11 that can include the

substrate material itself or an optional epitaxial grown semiconductor layer that can be formed thereon prior to forming the n+ subcollector 14.

[Para 47] The n+ subcollector 14 is formed by implanting n-type dopant atoms such as As or P using a conventional ion implantation process and conditions that are well known to those skilled in the art. The implant may be a blanket implant providing a continuous subcollector 14 throughout the entire substrate or a masked ion implantation process can be used to form a discrete subcollector within a specific portion of the substrate. One possible n-type dopant that can be employed is As which can be implanted at a doping dosage from about 1E14 to about 5E16 atoms/cm^2 and at an energy from about 20 to about 100 keV. Other dopant ions and/or implant conditions besides those mentioned above can also be employed. The n+ subcollector 14 is located about 300 to about 2000 nm from the upper surface of the substrate 12.

[Para 48] Notwithstanding the type of dopant used, the subcollector 14 typically has a dopant concentration from about 1E18 to about 1E20 atoms/cm^3, with a dopant concentration from about 1E19 to about 1E20 atoms/cm^3 being more typical.

[Para 49] Note that although the subcollector 14 is shown as being formed at this point of the present invention, the subcollector 14 can be formed latter on during the process, i.e., after isolation region formation, but prior to well region formation.

[Para 50] In some embodiments as mentioned above, an epitaxial semiconductor layer such as silicon or SiGe is formed on the surface of the semiconductor substrate 12 utilizing a conventional epitaxial growth process that is well known to those skilled in the art. This epitaxial layer would correspond to region 11 labeled in FIG. 1A.

[Para 51] Next, and as shown in FIG. 1B, a plurality of isolation regions 16 are formed into an upper region 11 of semiconductor substrate 12. The plurality of isolation regions 16 formed at this point of the present invention may be local oxidation of silicon (LOCOS) isolation regions, or more preferably, the plurality of isolation regions 16 are trench isolation regions, as shown in FIG. 1B. The isolation regions 16 are formed utilizing processes that are well known to those skilled in the art. For example, and when the isolation regions 16 are comprised of LOCOS isolation regions, a local oxidation of silicon process can be employed in forming such isolation regions. When the isolations regions 16 are comprised of trench isolation regions, the trench isolation regions are formed by lithography, etching and trench fill (i.e., deposition of a trench dielectric such as tetratethylorthosilicate (TEOS) or a high-density plasma oxide (HDPO)). A planarization process such as chemical mechanical polishing (CMP) or grinding may optionally follow the trench fill. Also, an optional densification process can be used.

[Para 52] In the present invention, the plurality of isolation regions 16 are formed in the upper region 11 of the substrate 12 and they do not extend down to the n+ subcollector 14. Two neighboring isolation regions, as shown in FIG. 1B, define device region 18.

[Para 53] Next, a well region of alternating conductivity is formed via ion implantation and annealing. In the present example depicted in FIG. 1C, the well region of alternating conductivity comprises first N-well region 20A, P-well region 20B, and second N-well region 20C. In another embodiment, the alternative doping configuration is formed for the well region. In the present example depicted in FIG. 1C, the P-well region ("active well") 20B is located in the device region 18. The N-well regions 20A and 20C are formed adjacent to device region 18 and those well regions can be referred to herein as "reach-through implant regions". As shown, the well regions extend beneath the isolation regions 16 such that each neighboring well region is in contact with

the adjoining well region, for example, 20A and 20B. The well regions 20A, 20B and 20C extend down to the surface of the n+ subcollector 14, as is depicted in FIG. 1C. The well regions 20A and 20C are used to electrically contact the subcollector 14 or isolation well 14.

[Para 54] As stated above, the well regions are formed by ion implantation and annealing. The type of dopant used in forming each well is dependent on the final polarity of the varactor. N-type dopants such as an element from Group VA of the Periodic Table of Elements like As and P are employed in forming the N-wells, while p-type dopants such as an element from Group IIIA of the Periodic Table of Elements like B, In and Ga are used in forming the P-well.

[Para 55] Notwithstanding the type of dopant used, each well region typically has a dopant concentration from about 1E17 to about 1E19 atoms/cm^3, with a dopant concentration from about 1E17 to about 1E18 atoms/cm^3 being more typical.

[Para 56] In accordance with the present invention, a selective dopant ion type is implanted into a portion of the semiconductor substrate 12 utilizing a masked ion implantation process. The outer well regions 20A and 20C can be formed at the same time utilizing the same implantation conditions. Alternatively, the outer well regions 20A and 20C can be formed at different times utilizing different implantation conditions. The order of the implantations may vary. For example, well region 20B can be formed before or after well regions 20A and 20C.

[Para 57] The implantation conditions used in forming each well region are conventional and are well known to those skilled in the art. For example, the implant conditions for forming a N-well region can include a n-type dopant dosage from about 1E12 to about 8E15 atoms/cm^2 and an energy from about

30 to about 1000 keV. The P-well region can be formed utilizing a p-type dopant dosage from about 1E12 to about 8E13 atoms/cm^2 and an energy from about 30 to about 600 keV. If a reach-through (n-type) implant is available in the technology, one would replace this implant for the standard N-well implants. Typically, this reach-through implant includes an n-type dopant such as Sb; dopant dosage is from 5E13 to 5E14 and an energy from 100 to 300 keV.

[Para 58] The ion implantations can be performed using a substantially vertical ion implantation process or alternatively, an angled ion implantation process can be used.

[Para 59] The annealing process is used to activate the dopants within each well region. A single annealing step can be used after the well region is formed, or alternatively, an anneal process can follow the implantation of each individual well region. The annealing temperature used in the present invention is typically from about 900°C or greater, with an annealing temperature from about 1000°C or greater being more typical. The annealing times may vary depending on the type of anneal process used. For example, annealing times of about 5 minutes or less are typically used for a rapid thermal anneal (RTA) process, a laser annealing, or a spike anneal, while annealing times of about 30 minutes or greater are typically used for furnace annealing.

[Para 60] It should be noted that the activation of the well regions can be delayed until another thermal cycle within the process of the present invention is performed. For example, the well regions can be activated during source/drain diffusion activation. Delaying the activation of the well regions until a latter thermal process is advantageous since it reduces the number of thermal cycles, and hence cost, within the overall process.

[Para 61] A conventional CMOS process is then employed providing the varactor 22 shown in FIG. 1D. Note that the varactor 22 shown in FIG. 1D comprises a field effect transistor (FET) which includes gate dielectric 24, gate conductor 26, at least one spacer 30 located on sidewalls of at least the gate conductor 26 and source/drain regions 32 located in the upper portion of substrate 10. The varactor 22 is located within the device region 18 atop the middle well region, i.e., P-well region 20B.

[Para 62] One conventional CMOS process that can be used in forming the varactor 22

[Para 63] shown in FIG. 1D includes the following steps: gate dielectric 24 is first formed on the entire surface of the structure shown in FIG. 1C including the semiconductor substrate 12 and atop the isolation regions 16, if they are comprised of a deposited dielectric.

[Para 64] The gate dielectric 24 can be formed by a thermal growing process such as, for example, oxidation, nitridation or oxynitridation. Alternatively, the gate dielectric 24 can be formed by a deposition process such as, for example, chemical vapor deposition (CVD), plasma-assisted CVD, atomic layer deposition (ALD), evaporation, reactive sputtering, chemical solution deposition and other like deposition processes. The gate dielectric 24 may also be formed utilizing any combination of the above processes.

[Para 65] The gate dielectric 24 is comprised of an insulating material including, but not limited to: an oxide, nitride, oxynitride and/or silicate including metal silicates and nitrided metal silicates. In one embodiment, it is preferred that the gate dielectric 24 is comprised of an oxide such as, for example, SiO_2, HfO_2, ZrO_2, Al_2O_3, TiO_2, La_2O_3, $SrTiO_3$, $LaAlO_3$, and mixtures thereof.

[Para 66] The physical thickness of the gate dielectric 24 may vary, but typically, the gate dielectric 24 has a thickness from about 0.5 to about 10 nm, with a thickness from about 0.5 to about 3 nm being more typical.

[Para 67] After forming the gate dielectric 24, a blanket layer of polysilicon (i.e., polySi) which becomes the gate conductor 26 shown in FIG. 1D is formed on the gate dielectric 24 utilizing a known deposition process such as, for example, physical vapor deposition, CVD or evaporation. The blanket layer of polysilicon may be doped or undoped. If doped, an in-situ doping deposition process may be employed in forming the same. Alternatively, a doped polySi layer can be formed by deposition, ion implantation and annealing. The doping of the polySi layer will shift the workfunction of the gate formed. Illustrative examples of dopant ions include As, P, B, Sb, Bi, In, Al, Ga, Tl or mixtures thereof. In the example shown in the drawings, a p-doped polysilicon gate conductor 26 is formed. Preferable doses for the ion implants are 1E14 ($=1x10^{14}$) to 1E16 ($=1x10^{16}$) atoms/cm^2 or more preferably 1E15 to 5E15 atoms/cm^2. The thickness, i.e., height, of the polysilicon layer deposited at this point of the present invention may vary depending on the deposition process employed. Typically, the polysilicon layer has a vertical thickness from about 20 to about 180 nm, with a thickness from about 40 to about 150 nm being more typical.

[Para 68] Notwithstanding the type of dopant used, the gate conductor 26 typically has a dopant concentration from about 1E19 to about 1E21 atoms/cm^3, with a dopant concentration from about 5E19 to about 5E20 atoms/cm^3 being more typical.

[Para 69] After deposition of the blanket layer of polysilicon 26, a hard mask 28 is formed atop the blanket layer of polysilicon 26 utilizing a deposition process such as, for example, physical vapor deposition or chemical vapor deposition. The hard mask 28 may be an oxide, nitride, oxynitride or any

combination thereof. In one embodiment, a nitride such as, for example, Si_3N_4, is employed as the hard mask 28. In yet another embodiment, the hard mask 28 is an oxide such as SiO_2. The thickness, i.e., height, of the hard mask 28 is from about 20 to about 180 nm, with a thickness from about 30 to about 140 nm being more typical.

[Para 70] The blanket polysilicon layer 26 and the hard mask 28 are then patterned by lithography and etching so as to provide at least one patterned gate stack. The patterned gate stacks may have the same dimension, i.e., length, or they can have variable dimensions to improve device performance. Each patterned gate stack at this point of the present invention includes the polySi gate conductor 26 and the hard mask 28. The lithography step includes applying a photoresist to the upper surface of the hard mask 28, exposing the photoresist to a desired pattern of radiation and developing the exposed photoresist utilizing a conventional resist developer. The pattern in the photoresist is then transferred to the hard mask 28 and the blanket layer of polysilicon 26 utilizing one or more dry etching steps. In some embodiments, the patterned photoresist may be removed after the pattern has been transferred into the hard mask 28. In other embodiments, the patterned photoresist is removed after etching has been completed.

[Para 71] It is noted that the hardmask 28 is typically removed during or after the gate patterning process. The hardmask 28 is not typically present in the final structure. See FIG. 1D.

[Para 72] Suitable dry etching processes that can be used in the present invention in forming the patterned gate stack include, but are not limited to: reactive ion etching, ion beam etching, plasma etching or laser ablation. The dry etching process employed is typically selective to the underlying gate dielectric 24 therefore this etching step does not typically remove the gate dielectric 24. In some embodiments, this etching step may however be used

to remove portions of the gate dielectric 24 that are not protected by the gate stack.

[Para 73] Next, at least one spacer 30 is formed on exposed sidewalls of the patterned gate stack. The at least one spacer 30 is comprised of an insulator such as an oxide, nitride, oxynitride and/or any combination thereof. The at least one spacer is formed by deposition and etching.

[Para 74] The width of the at least one spacer 30 must be sufficiently wide enough such that the source and drain silicide contacts (to be subsequently formed) do not encroach underneath the edges of the gate stack. Typically, the source/drain silicide does not encroach underneath the edges of the gate stack when the at least one spacer 30 has a width, as measured at the bottom, from about 15 to about 80 nm.

[Para 75] After spacer formation, source/drain regions 32, 32' are formed into the substrate 12. The source/drain regions 32, 32' are formed utilizing ion implantation and an annealing step. The annealing step serves to activate the dopants that were implanted by the previous implant step. The conditions for the ion implantation and annealing are well known to those skilled in the art. The term "source/drain regions" includes deep source/drain diffusion regions, optional halo implants and source/drain extension regions.

[Para 76] Next, and if not previously removed, the exposed portion of the gate dielectric 24 is removed utilizing a chemical etching process that selectively removes the gate dielectric 24. This etching step stops on an upper surface of the semiconductor substrate 12 as well as an upper surface of the isolation regions 16. Although any chemical etchant may be used in removing the exposed portions of the gate dielectric 24, in one embodiment dilute hydrofluoric acid (DHF) is used.

[Para 77] The source/drain regions 32, 32' and optionally at least a portion of gate conductor 24 can be silicided at this point of the present invention by utilizing a conventional source/drain silicidation process and metal gate silicidation processes that are well known to those skilled in the art.

[Para 78] It is noted that FIG. 1D shows the structure of the present invention for BiCMOS or bipolar applications, i.e., varactor 22 located atop a substrate 12 that includes a well scheme and an underlying subcollector. In the drawing, the varactor 22 includes a p-type polysilicon gate conductor 26, an underlying P-well region 20B, adjacent N-well regions 20A and 20C that are separated from the varactor by isolation regions 16 and underlying n+ subcollector 14 which isolates the P-well region 20B from the body of the p-type semiconductor substrate 12. The opposite polarity type of structure is also contemplated, i.e., a n-type polysilicon gate conductor 26, an underlying N-well region 20B, adjacent P-well regions 20A and 20C that are separated from the varactor structure by isolation regions 16 and underlying p+ subcollector 14 which isolates the N-well region 28B from the body of the n-type semiconductor substrate 12.

[Para 79] The structure depicted in FIG.1D is preferred since it provides a negative bias accumulation varactor that operates in depletion.

[Para 80] It is noted that other varactors 22 can be formed on the surface of the substrate 12 as needed.

[Para 81] FIG. 2 shows the CV characteristics of a prior art NMOS in a N-well (Curve 1), a prior art PMOS in a P-well (Curve 2) and the inventive varactor PMOS in a P-well with a well scheme and an underlying n+ subcollector or isolation well. One observes from this drawing that the minimum capacitance

on the inventive varactor decreases and thus increases the tunability of the device in comparison to curves 1 and 2. This decrease in minimum capacitance is an affect of the slight counterdoping of the n-type subcollector or the isolation well. This decreases the inventive p-type dopants in the P-well and therefore reduces the minimum capacitance.

[Para 82] FIGS. 3A-3C illustrate the processing steps used in forming a varactor for CMOS applications. The process begins by first providing the structure shown in FIG. 3A which includes a semiconductor substrate 12 having a plurality of isolation regions 16 formed into an upper region of the substrate 12. The plurality of isolation regions 16 are formed as described above. As shown, device region 18 forms between two neighboring isolation regions. The semiconductor substrate 12 is doped with a first conductivity type dopant (n- or p-type).

[Para 83] Next, isolation well 14 (i.e., dopant region of second conductivity type) is formed by ion implanting a p- or n-type dopant into the structure shown in FIG. 3A producing the structure shown in FIG. 3B. The isolation well region 14 is formed utilizing conventional implantation processes that are well known to those skilled in the art.

[Para 84] Next, well regions 20A, 20B and 20C are formed as described above. Note that 20A and 20C are reach-through implants that have the same conductivity type dopant as the isolation well region 14, while active well region 20B has the same conductivity type dopant as the substrate. The resultant structure is shown in FIG. 3C.

[Para 85] Further processing as described above, can be formed on the structure shown in FIG. 3C so as to provide the structure shown in FIG. 1D.

[Para 86] While the present invention has been particularly shown and described with respect to preferred embodiments thereof, it will be understood by one skilled in the art that the foregoing and other changes in forms and details may be made without departing from the spirit and scope of the invention. It is therefore intended that the present invention is not limited to the exact forms and details described and illustrated, but falls within the spirit and scope of the appended claims.